REMARKS

Claims 1-19 were pending in the application. Claim 19 has been cancelled. Claims 1-18 have been amended. Claim 20 is newly submitted. The specification has been amended to correct informalities. No new matter has been added. Accordingly, claims 1-18 and 20 remain pending in the application. Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks.

I. Title

The title of the invention has been cited as not descriptive. Accordingly, Applicant has amended the title to read "Method and Apparatus for Dynamically Programming a Field Programmable Gate Array (FPGA) in a Coprocessor." Applicant respectfully submits that the new title is descriptive of the invention.

II. The §102 Rejections

Claims 1-19 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,721,884 ("Pereira").

Claim 1, as amended, recites a method for dynamically programming a field programmable gate array (FPGA) in a coprocessor. In particular, the method includes providing a processor and a coprocessor that is separate from the processor. The coprocessor is coupled to the processor and includes a field programmable gate array (FPGA). The field programmable gate array (FPGA) is dynamically programmed to perform a function responsive to a determination that the field programmable gate array (FPGA) is not programmed to perform the function.

Pereira discloses a processor including a configurable functional unit that is capable of executing reconfigurable instructions. The configurable functional unit can be reconfigured at

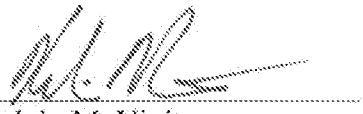
run-time (see Abstract). Pereira, however, fails to disclose providing a coprocessor that is separate from a processor, in which the coprocessor is coupled to the processor and includes a field programmable gate array (FPGA), as recited in claim 1. Instead, Pereira discloses only providing a processor that includes a configurable functional unit (see FIG. 1). Pereira fails to disclose a coprocessor coupled to the processor, or a coprocessor that includes a field programmable gate array (FPGA). Claim 1 is, therefore, allowable over Pereira.

Claims 2-8 depend from claim 1, and are allowable for at least the reasons that apply to claim 1.

Independent claims 9, 10, 18 and 20 (and the claims that depend therefrom) incorporate limitations similar to claim 1, and are also allowable for at least the reasons that apply to claim 1.

Applicant submits that claims 1-18 and 20 are allowable over the reference cited above, and are in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call the undersigned at the telephone number indicated below.

Respectfully submitted,
SAWYER LAW GROUP LLP



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